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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,990	02/09/2004	Matthew J. Amatangelo	P8900	9588

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EXAMINER	
PATEL, SHAMBHAVI K	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,990	AMATANGELO ET AL.	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 28 May 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS as to the merits.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 1-5, 7, and 17 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The specification defines a "near domino function" as "propagating the data signal as an output when the output of the combinatorial gate corresponds to the data." **([0009]).** It is unclear how, in **claim 1**, propagating the data signal models a near domino function if by definition a near domino function propagates the data signal. It is unclear how, in **claim 7**, "modeling the output of the combinatorial gate as a data signal includes a near domino function" if "modeling the output of the combinatorial gate as a data signal when an input to the next element of the circuit is a data signal" (from **claim 6**) is by definition a near domino function. It is unclear how, in **claim 17**, the means for modeling the output of the combinatorial gate as a data signal *includes* means for modeling a near domino function if the two are equivalent by definition. All other claims are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. **Claims 1-20 are rejected under 35 U.S.C. 101** because the claimed invention is directed to non-statutory subject matter. The Examiner asserts that the current state of the claim language is such that a reasonable interpretation of the claims would not result in any useful, concrete or tangible product. **Claim 1** is directed to a method of modeling a combinatorial gate. **Claim 6** is directed to a method of determining how to model a combinatorial gate where the combinatorial gate receives a data signal and a clock signal. **Claim 11** is directed to a method of modeling a combinatorial gate within a static timing analysis. **Claim 16** is directed to a static time engine. This claimed subject matter lacks a practical application of a judicial exception (law of nature, abstract idea, naturally occurring article/phenomenon) since it fails to produce a useful, concrete and tangible result. Specifically, the claimed subject matter does not produce a tangible result because the claimed subject matter fails to produce a result that is limited to having real world value rather than a result that may be interpreted to be abstract in nature as, for example, a thought, a computation, or manipulated data. More specifically, the claimed subject matter provides for propagating/modeling the data signal as an output when the output of the combinatorial gate corresponds to a data signal **(claims 1 and 6)**, providing an output having a near domino function **(claim 11)** and means for modeling the output of the combinatorial gate as a data signal **(claim 16)**. This produced results remain in the abstract and, thus, fail to achieve the required status of having real world values. **Claim 16** is not statutory because it is software, per se. There is no evidence that the components of the timing engine are anything more than program modules. All other claims are rejected by virtue of dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claim 1-20 are rejected under 35 U.S.C. 102(b)** as being clearly anticipated by **Rajsuman (US Patent No. 5,867,036).**

Regarding claim 1:

Rajsuman discloses a method of modeling a combinatorial gate comprising:

a. providing a data signal input at the combinatorial gate **(figure 6 data inputs 86)**

b. providing a clock signal input at the combinatorial gate **(figure 6 clock input 126, domino clock)**

c. propagating the clock signal as an output signal when the output of the combinatorial gate corresponds to the clock signal and propagating the data signal as an output when the output of the combinatorial gate corresponds to the data signal, the propagating the data signal modeling a near domino function **(column 7 lines 11-23)**. When the domino clock is 0, the domino logic is being initialized, and the output is 0 (equivalent to the clock input). When the domino clock is 1, the evaluation phase is entered, and the test vector (data input) is applied to the domino logic and the response (output) is stored in the register.

Regarding claim 2:

Rajsuman discloses the method of claim 1 wherein the near domino function is propagated based upon performing a reverse traversal function on a circuit design containing the combinatorial gate **(column 6 lines 32-38)**.

Regarding claim 3:

Rajsuman discloses the method of claim 1 wherein: the near domino function includes causing a later arriving edge of the data signal to cause the output signal to respond **(column 6 lines 2-6)**.

Regarding claim 4:

Rajsuman discloses the method of claim 1 wherein: the data signal includes a single edge per clock period and when providing the near domino function, the single edge is propagated through the combinatorial gate **(column 6 lines 54-59)**.

Regarding claim 5:

Rajsuman discloses the method of claim 1 wherein: the clock signal includes two edges per clock period; and, when propagating the clock signal, the two edges are propagated through the combinatorial gate **(column 7 lines 2-10)**. The minimum period that the clock can be low can be selected.

Regarding claim 6:

Rajsuman discloses a method of determining how to model a combinatorial gate where the combinatorial gate receives a data signal and a clock signal comprising:

a. performing a reverse traversal function on a circuit containing the combinatorial gate **(column 6 lines 32-38)**

b. modeling an output of the combinatorial gate as the clock signal when an input to a next element of the circuit is a clock and modeling the output of the combinatorial gate as a data signal when an input to a next element of the circuit is a data signal **(column 7 lines 11-23)**. When the domino clock is 0, the domino logic is being initialized, and the output is 0 (equivalent to the clock input). When the domino clock is 1, the evaluation phase is entered, and the test vector (data input) is applied to the domino logic and the response (output) is stored in the register.

Regarding claim 7:

Rajsuman discloses the method of claim 6 wherein: the modeling the output of the combinatorial gate as a data signal includes a near domino function **(column 7 lines 11-23)**.

Regarding claim 8:

Rajsuman discloses the method of claim 7 wherein: the near domino function includes causing a later arriving edge of the data signal to cause the output signal to respond **(column 6 lines 2-6)**.

Regarding claim 9:

Rajsuman discloses of claim 7 wherein: the data signal includes a single edge per clock period; and, when providing the near domino function, the single edge is propagated through the combinatorial gate **(column 6 lines 54-59)**

Regarding claim 10:

Rajsuman discloses the method of claim 7 wherein: the clock signal includes two edges per clock period; and, when propagating the clock signal, the two edges are propagated through the

combinatorial gate **(column 7 lines 2-10).** The minimum period that the clock can be low can be selected

Regarding claim 11:

Rajsuman discloses a method of modeling a combinatorial gate within a static timing analysis comprising:

a. receiving a data signal at the combinatorial gate **(figure 6 data inputs 86)**

b. receiving a clock signal at the combinatorial gate **(figure 6 clock input 126, domino clock)**

c. providing an output corresponding to the clock signal when the output of the combinatorial gate corresponds to the clock signal and providing an output having a near domino function when the output of the combinatorial gate corresponds to the data signal **(column 7 lines 11-23).**. When the domino clock is 0, the domino logic is being initialized, and the output is 0 (equivalent to the clock input). When the domino clock is 1, the evaluation phase is entered, and the test vector (data input) is applied to the domino logic and the response (output) is stored in the register.

Regarding claim 12:

Rajsuman discloses the method of claim 11 wherein: the near domino function is provided based upon performing a reverse traversal function on a circuit design containing the combinatorial gate **(column 7 lines 11-23).**

Regarding claim 13:

Rajsuman discloses the method of claim 11 wherein: the near domino function includes causing a later arriving edge of the data signal to cause the output signal to respond **(column 6 lines 2-6).**

Regarding claim 14:

Rajsuman discloses the method of claim 11 wherein: the data signal includes a single edge per clock period; and, when providing the near domino function, the single edge is propagated through the combinatorial gate **(column 6 lines 54-59)**.

Regarding claim 15:

Rajsuman discloses the method of claim 11 wherein: the clock signal includes two edges per clock period; and, when providing the clock signal as the output, the two edges are propagated through the combinatorial gate **(column 7 lines 2-10)**. The minimum period that the clock can be low can be selected

Regarding claim 16:

Rajsuman discloses the static timing engine comprising:

a. a data model, the data model including a combinational block determinator module, the combinational block determinator module including means for performing a reverse traversal function on a circuit containing the combinatorial gate **(column 6 lines 32-38)**.

b. timing engine portion coupled to the data model, the timing engine portion including means for modeling an output of the combinatorial gate as a clock signal when an input to a next element of the circuit is clock input; and, means for modeling the output of the combinatorial gate as a data signal when an input to a next element of the circuit is a data input **(column 7 lines 11-23)**. When the domino clock is 0, the domino logic is being initialized, and the output is 0

(equivalent to the clock input). When the domino clock is 1, the evaluation phase is entered, and the test vector (data input) is applied to the domino logic and the response (output) is stored in the register.

Regarding claim 17:

Rajsuman discloses the static timing engine of claim 16 wherein: the means for modeling the output of the combinatorial gate as a data signal includes means for modeling a near domino function (column 7 lines 11-23).

Regarding claim 18:

Rajsuman discloses the static timing engine of claim 17 wherein: the near domino function includes causing a later arriving edge of the data signal to cause the output signal to respond **(column 6 lines 2-6)**.

Regarding claim 19:

Rajsuman discloses the static timing engine of claim 17 wherein: the data signal includes a single edge per clock period; and, when providing the near domino function, the single edge is propagated through the combinatorial gate **(column 6 lines 54-59)**.

Regarding claim 20:

Rajsuman discloses the static timing engine of claim 17 wherein: the clock signal includes two edges per clock period; and, when propagating the clock signal, the two edges are propagated through the combinatorial gate **(column 7 lines 2-10)**. The minimum period that the clock can be low can be selected

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKP

KAMINI SHAH
SUPERVISORY PATENT EXAMINER